transmitting a first digital signal from the memory device to the memory controller according to the initial output timing;

receiving the first digital signal at the memory controller;

identifying a phase difference of the received digital signal relative to a timing reference signal;

transmitting an adjustment signal from the memory controller to the memory device for revising the initial output timing in response to the identified phase difference to produce a revised output timing;

revising the initial output timing at the memory device according to the adjustment signal; and

transmitting a second digital signal from the memory device to the memory controller according to the revised output timing.

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21. The method of claim 20 wherein the step of identifying a phase difference of the received first digital signal relative to a timing reference signal comprises the steps of:

generating a plurality of phase shifted signals responsive to the timing reference signal;

comparing the first digital signal to each of the phase shifted signals; and

identifying one of the phase shifted signals having a phase within a selected range of phases relative to the first digital signal.

22. The method of claim 20 wherein the step of establishing an initial output timing includes the steps of:

setting a delay of a delay circuit; and

applying the timing reference signal to the delay circuit to produce the first digital signal.

23. The method of claim 22 wherein the step of establishing an initial output timing further includes the steps of: